What is Claimed is:

1. A method of forming a double gate electrode comprising:

forming a tunnel structure in an active region of a substrate that is defined by a trench positioned in an isolation region of the substrate, the tunnel structure extending substantially parallel to the substrate;

forming a first insulation layer inside the tunnel structure and inside the trench;

forming a bottom gate electrode on the first insulation layer inside the tunnel structure, the bottom gate electrode extending into the trench;

forming a second insulation layer on the active region of the substrate; and

forming a top gate electrode on the second insulation layer opposite the tunnel structure.

2. The method of Claim 1, wherein the substrate comprises silicon and wherein forming the tunnel structure further comprises:

forming a dummy bottom gate pattern on a bottom gate region of the substrate using a material having etching selectivity of more than about 1:10 relative to silicon;

forming a silicon channel layer on the substrate having the dummy bottom gate pattern;

forming the trench to expose the dummy bottom gate pattern by sequentially etching the silicon channel layer and the substrate; and

forming the tunnel structure by selectively etching the dummy bottom gate pattern.

3. The method of Claim 2, wherein the dummy bottom gate pattern includes $Si_{1-X}Ge_X$ wherein $0<X$ 1.

4. The method of Claim 3, wherein the X is in a range of about 0.01 to about 0.5.

5. The method of Claim 2, wherein the dummy gate pattern has a line shape.

6. The method of Claim 2, wherein forming the dummy bottom gate pattern further comprises:

forming a first mask pattern partially exposing the bottom gate region;

etching the substrate using the first mask pattern as an etching mask;

forming a silicon-germanium pattern by epitaxially growing silicon-germanium from the etched portion of the substrate; and

removing the first mask pattern.

7. The method of Claim 6, wherein the substrate is etched to a depth of about 50Å to about 2,000Å.

8. The method of Claim 2, wherein the silicon channel layer is formed by epitaxially growing silicon from the substrate.

9. The method of Claim 2, wherein forming the trench further comprises:

forming a second mask pattern on the silicon channel layer to mask the active region; and

etching the silicon channel layer and the substrate using the second mask pattern as an etching mask.

10. The method of Claim 9, wherein the second mask pattern includes silicon nitride.

11. The method of Claim 2, wherein selectively etching the dummy bottom gate pattern is performed using a wet etching process and/or a dry etching process.

12. The method of Claim 1, wherein the first insulation layer has a thickness of about 10Å to about 100Å.

13. The method of Claim 1, further comprising partially filling an insulation material in the trench before forming the bottom gate electrode.

14. The method of Claim 13, wherein partially filling the insulation material comprises:

forming a third insulation layer to fill up the trench; and

etching the third insulation layer so that the third insulating layer partially remains in a portion of the trench beneath the bottom gate region while the first insulation layer remains on the tunnel structure.

15. The method of Claim 13, wherein partially filling the insulation material comprises:

forming a third insulation layer to fill up the trench;

etching the third insulation layer so that the third insulation layer remains at a portion of the trench beneath the bottom gate region, wherein the first insulation layer on the tunnel structure is simultaneously etched; and

forming a bottom gate oxide layer on the bottom gate region and in the trench structure.

16. The method of Claim 15, wherein the bottom gate oxide layer has a thickness of about 10Å to about 100Å.

17. The method of Claim 1, wherein forming the bottom gate electrode further comprises:

forming a conductive layer by depositing conductive material in the tunnel structure and on the substrate;

etching the conductive layer so that the conductive layer remains in the tunnel structure;

forming a fourth insulation layer on the substrate including the conductive layer;

polishing the fourth insulation layer and the conductive layer so that the fourth insulation layer and the conductive layer remain in the trench structure; and

etching the conductive layer in the trench structure so that the conductive layer fills up the tunnel structure and extends into the trench.

18. The method of Claim 17, wherein the conductive material includes at least one material selected from the group consisting of polysilicon, tungsten, tungsten silicide, titanium silicide, titanium nitride and tungsten nitride.

19. The method of Claim 17, wherein etching the conductive layer further comprises:

forming an insulation material to fill the trench; and

polishing the insulation material so that the insulation material remains in the trench.

20. The method of Claim 1, further comprising, after forming the bottom gate electrode:

forming an insulation material to fill the trench.

21. The method of Claim 1, wherein the bottom gate electrode and the top gate electrode are fabricated to have substantially identical resistance by adjusting lengths of the bottom and the top gate electrodes and/or varying materials included in the bottom and the top gate electrodes.

22. A method of Claim 1, further comprising:

forming source and drain regions by implanting impurities into the substrate;

forming a bit line electrically connected to the source region; and

forming a capacitor electrically connected to the drain region.

23. A method of forming a double gate electrode for a field effect transistor comprising:

forming in a substrate, a trench and a tunnel that extends from a sidewall of the trench parallel to the substrate;

forming an insulating coating inside the tunnel;

forming a bottom gate electrode within the insulating coating inside the tunnel;

forming an insulating layer on the substrate; and

forming a top gate electrode on the insulating layer opposite the bottom gate electrode.

24. The method of Claim 23, wherein forming in the substrate, the trench and the tunnel that extends from a sidewall of the trench parallel to the substrate, comprises:

forming a dummy bottom gate on the substrate;

forming a semiconductor channel region on the dummy bottom gate;

forming a trench that extends through a portion of the semiconductor channel region and the dummy bottom gate; and

etching the dummy bottom gate to define the tunnel.

25. The method of Claim 24, wherein the substrate comprises a first semiconductor and wherein forming the dummy bottom gate comprises:

forming a bottom gate trench in the substrate; and

epitaxially growing a second semiconductor into the bottom gate trench from the first semiconductor.

26. The method of Claim 25, wherein forming the semiconductor channel region on the dummy bottom gate comprises epitaxially growing the first semiconductor on the second semiconductor.

27. The method of Claim 25, wherein the first semiconductor comprises a single element semiconductor and wherein the second semiconductor comprises a compound semiconductor.

28. The method of Claim 23, wherein the following is performed prior to forming the bottom gate electrode:

filling the trench up to a floor of the tunnel; and

wherein forming the bottom gate electrode comprises:

forming the bottom gate electrode within the insulating coating inside the tunnel and on the trench that is filled up to the floor of the tunnel.